Research on the delay-line readout for GEM detectors*

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Abstract Based on the principles of transmission line and the output signal of GEM detector, a full simulation model of delay-line circuit has been described in this paper. The consistency of simulation results and experimental data shows that the method is very effective for the design of delay-line readout.

Key words GEM, delay-line readout, particle detector

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1 Introduction

Recently, GEM (Gas Electron Multiplier) -based detectors opened a new trend in the domain of X-ray imaging[1—3]. GEM consists of a thin copper-clad Kapton foil with a high density of holes (Fig. 1), typically with 50∼ 70 μm diameter and 140 μm pitch. On application of a working voltage between the two sides of the foil, the holes can focus the field lines and produce avalanche processes for charged particles[4]. A single layer GEM can reach gains in excess of 10^2, and a triple-layer GEMs can be assembled in cascade to provide more than 10^5 gains. Due to its special structure, the GEM-based detector has high spatial resolution and endured with high counter rate.

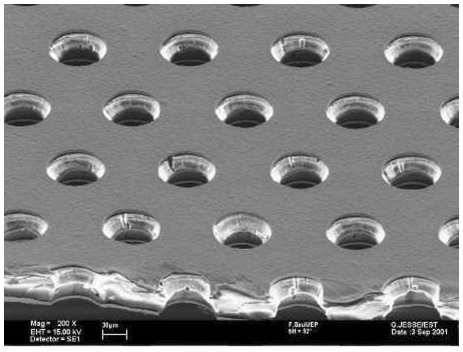

Fig. 1. GEM microscopic view.

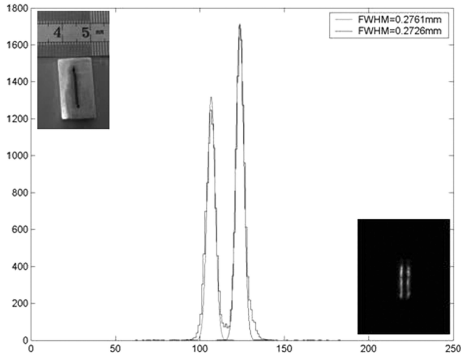

Fig. 2. X-ray image with COG method.

Typically, a prototype X-ray imaging GEM detector based on Center-of-Gravity(COG) readout method can achieve a good spatial resolution (∼ 70 μm, Fig. 2)[5], but the cost of the channel-by-channel readout is quite high which is not suitable for the application in X-ray imaging.

To decrease the cost on electronics and keep good spatial resolution, a new method for delay-line readout for GEM detector was studied. The simulation and experimental results showed that the design method is very effective.

2 Principle and model

A electric model of delay-line, based on the principle of transmission line[6], is shown in Fig. 3. The

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delay-line consists of discrete inductors and capacitors are soldered on a print circuit board (PCB) substrate. Three parameters: the per-cell delay time τ, characteristic impedance Z_0, cut-off frequency ω_0, are most important for a delay-line PCB design. An ideal delay-line can put off the input signal a certain time without any distortion. These parameters can be calculated by the inductance (L) and capacitance (C) of the elements:

$$\omega_0 = \frac{1}{\sqrt{LC}} \ , \tag{1}$$

$$Z_0 = \frac{1}{\sqrt{1-\left(\frac{\omega}{\omega_0}\right)^2}}\sqrt{\frac{L}{C}} \approx \sqrt{\frac{L}{C}}, \quad (\omega \ll \omega_0) \ , \tag{2}$$

$$\tau = \frac{1}{\omega}\left[\frac{\omega}{\omega_0}+\frac{1}{3}\left(\frac{\omega}{\omega_0}\right)^3+\cdots\right] \approx \sqrt{LC} \ , (\omega \ll \omega_0) \ . \tag{3}$$

When the delay-line is coupled on a detector and connected to each readout channel, the position information is converted into the time difference between signals. The linear dependence between the time difference and the position is determined by the time delay per cell which could be calculated according to Eq. (3).

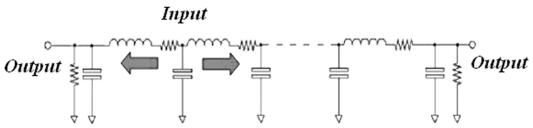

Fig. 3. Electric model of delay-line.

3 Simulation and experiment

According to the model of delay-line and the typical tested signals of GEM detector, three delay-line PCBs with different parameters are chosen for both the simulation and the experiment. The parameters are shown in Table 1, where R is the intrinsic inductor resistance. The cut off frequencies of all the delay-line PCBs are large enough so that the output signal of GEM detector can pass through with almost no distortion.

In Matlab-Simulink environment[7], a simulation program containing delay-line, Constant-fraction discriminator (CFD), and Time-Digital converter(TDC) (Shown in Fig. 4) was developed. Each simulated delay-line PCB contains 96 cells. The input signal (a trapeziform pulse with 40 ns width, 3 ns rising time and 0.75 V amplitude) injected into the delay-line at a certain cell port will propagate in opposite directions along the delay-line. The two sub-signals are eventually fed out at two output ports of the delay-line. The time difference between the two output signals is measured by CFD and TDC, which is shown on one LED panel. The amplitudes of output signals could also be recorded and shown on other two panels.

Table 1. Parameters of 3 kinds of delay line.

L/nH	R/Ω	C/pF	τ/ps	Z_0/Ω	ω_0/GHz
15	0.13	6	300	50	3.3
20	0.16	8	400	50	2.56
30	0.23	12	600	50	1.67

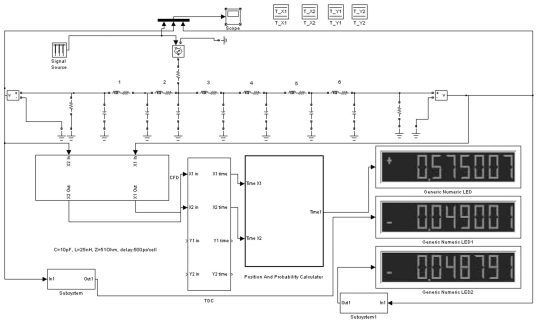

Fig. 4. Circuit diagram of simulation.

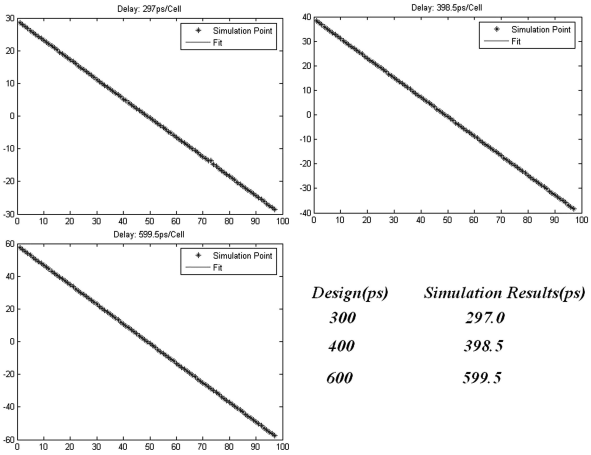

Fig. 5. Delay time vs signal input.

Figure 5 shows the simulation graphs of per cell delay time. As the effect of the intrinsic inductor resistance, there are little differences between the simulation results and the design values. Fig. 6 shows the amplitudes of output signals on left port versus the input position. The amplitude is maximal when input position is cell 1 and minimal when input position is cell 96. The ratios Min/Max of the three kinds of delay-line are: 0.86, 0.83, and 0.73 respectively.

Figure 7 shows the real print circuit board of

delay-line. The calibration data of these three delay-lines are shown in Table 2.

The difference between each pair of simuation and calibration results implies that the effect of PCB route must be considered. It's well known that the parasitical inductance and capacitance of route could remarkably shift the signal propagation capability of the delay-line. The parasitical capacitance is the most important parameter and it's evaluated by a modified

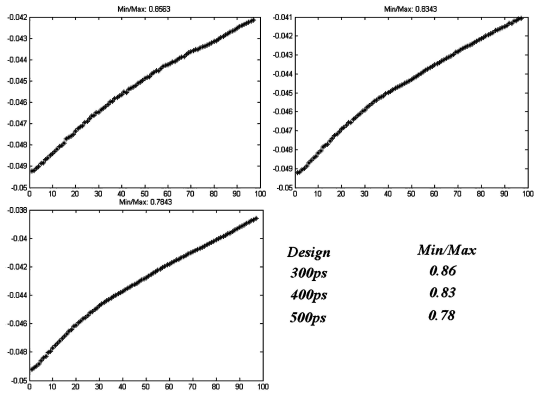

Fig. 6. Amplitude vs signal input position.

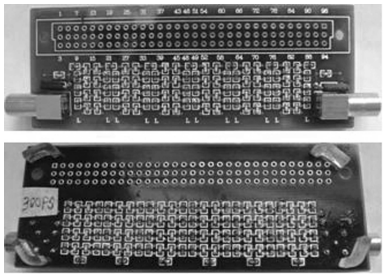

Fig. 7. Delay-line PCB.

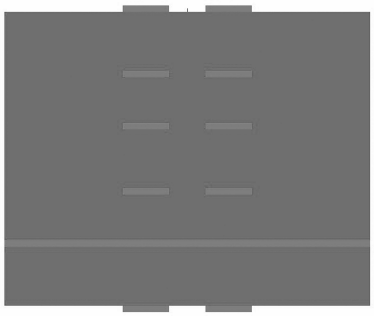

Fig. 8. Model of PCB in Ansoft 2D Extractor.

simulation model. Fig.8 shows the model in Ansoft 2D Extractor software[8]. The calculation of the parasitical capacitance for each layer of the multi-layer PCB is based on this model. The data from simulation are shown in Table 3. An average value of 2.3 pF/cell for parasitical capacitance is derived for each route. The new delay times based on the modified model are shown in Table 4, the simulation results are in good agreement with the calibration data.

Table 2. Simulation and calibration results.

design results	300ps	400ps	600ps
simulation results	297.0ps	398.5ps	599.5ps
calibration results	360.8ps	458.6ps	654.7ps

Table 3. Parasitical capacitance of PCB route (pF/m).

TopLayer	MidLayer1	MidLayer2	MidLayer3	Bottom-Layer
76.35	145.78	149.73	155.13	80.99

Table 4. Simulation results of modified model.

Ideal Design Value	Simulation results of new Model	Experiment results
300 ps	353.1 ps	360.8 ps
400 ps	454.9 ps	458.6 ps
600 ps	656.8 ps	654.7 ps

4 Conclusions

According to the model of delay-line circuit and the output signal of GEM detector, A full simulation model of delay-line readout system, containing the delay-line readout PCB, the amplifier, constant-fraction discriminator and the Time-Digital converter, is developed in Matlab-Simulink environment. Compared with the ideal model of delay-line and test results of the real delay-line PCBs, one actual model of delay-line circuit was constructed by taking into account of the affects of parasitical parameters of PCB route. The time delays of the PCB routes were calculated by the 2D Extractor of Ansoft Corporation. Designed three delay lines with new model, the rate of time delay are 353.1 ps/cell, 454.9 ps/cell, and 656.8 ps/cell, respectively , which are in good agreement with experiment results.

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