Design of a low level radio frequency control system for the direct current-superconductive photocathode injector at Peking University*

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Abstract: A digital low level radio frequency (LLRF) control system based on a high precision field-programmable gate array (FPGA) is being developed for the stable operation of the upgraded direct current-superconductive (DC-SC) photocathode injector at Peking University. The design of this LLRF control system is described, including both the hardware and the internal algorithm. Analysis of disturbances shows that the system can achieve the requirement of ±0.1% for amplitude stability and ±0.1° for phase stability. Through experiments, preliminary results are presented in the paper.

Key words: injector, LLRF, detuning sources, FPGA

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1 Introduction

The DC-SC photocathode injector developed by Peking University is a low emittance, high brightness electron beam source. The concept is to integrate a Pierce DC gun and a superconducting cavity to solve the compatibility of the photocathode and the superconducting cavity [1]. A prototype photocathode injector with a Pierce gun and a 1.5 cell superconducting cavity was manufactured in 2002，and the feasibility of the DC-SC photocathode injector was demonstrated by beam experiments in 2004 [2]. Recently, the DC-SC photocathode injector has been upgraded with a 3.5 cell superconducting cavity made of large-grain-size niobium sheets and working at 2K (Fig. 1). This cavity has been tested in JLab and the accelerating gradient $E_{\rm acc}$ and Q_0 value reached 23.5 MV/m and 1.2×10^{10}, respectively [3]. The $Q_{\rm ext}$ of the main coupler is set at 1.2×10^7 and the bunch repetition of the electron beam for the upgraded injector is 81.25 MHz. Such a design is required in order to meet the research and development requirements of the Peking University Energy Recovery Linac (PKU-ERL) and Free Electron Laser (PKU-FEL) [4]. In order to maintain the stability of the electromagnetic field in the 3.5 cell cavity, a digital low level RF control system based on FPGA is being developed for this upgraded injector with a precise control capability of ±0.1% for amplitude stability and ±0.1° for

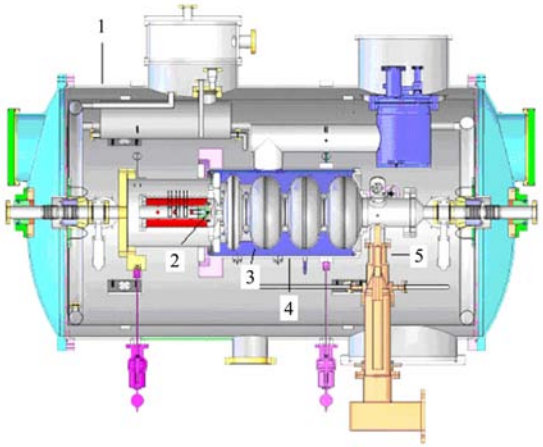

Fig. 1. The PKU SRF 3.5 cell photocathode injector. 1. Cryomodule, 2. Photocathode (Cs_2Te), 3. 3.5 cell LG Nb cavity, 4. Liquid helium tank, 5. Main coupler.

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phase stability. In this paper, the design of an LLRF system for the upgraded DC-SC injector is described, including both the hardware and the internal algorithm. Disturbances influencing system precision are analyzed and the preliminary results are presented in the paper.

2 Detuning instabilities of a 3.5 cell cavity

The microphonic beam loading effect and the Lorentz force are the main detuning instabilities affecting SRF accelerators. Therefore, the LLRF control system is very important for the stable operation of accelerator systems based on SRF technology.

Microphonics result from the mechanical vibrations of the surrounding environment and it is stochastic [5]. Beam loading effects, which widely exist in high energy accelerators, are caused by the field excited by the beam. Lorentz force detuning results from certain radiation pressures generated by an RF electromagnetic field, which produces effects on the SRF cavity surface and causes it to deform [6].

Considering that the 3.5 cell cavity will be operated on 10 MV/m, such a gradient does not reach the threshold value of Lorentz force (usually 15–20 MV/m) and the designed average beam current at the first step is about 1mA, the influence of Lorentz force and beam loading effect are not very important [7].

Microphonics is the main detuning instability in the 3.5 cell superconducting cavity in the DC-SC photocathode injector, which has thin shell construction. The main sources of it are the vibrations from assistant equipment such as the liquid helium and water cooling systems. Even though stiffening ring is used to prevent the cavity from being deformed [6], the LLRF control system is needed for further tuning.

The relationship between the detuning angle φ and the frequency variation can be presented as Formula (1),

$$\tan\varphi = 2Q_{\rm L}\frac{\Delta\omega_0}{\omega_0}, \tag{1}$$

here $Q_{\rm L}$ is load quality factor.

For the DC-SC injector system, $Q_{\rm L} = 1.2\times10^7$. If the frequency variation caused by microphonics is 5 Hz, the detuning angle would be 5.27°. It is important for the stable operation of our injector with a 3.5 cell cavity.

3 The design of LLRF control system

Compared with some analog systems with the precision of ±1% for amplitude and of ±1° for phase, the digital LLRF control system has advantages of high precision and a flexible algorithm. Therefore, we choose a digital technique to meet the high requirement of the DC-SC injector at Peking University. The schematic of the digital LLRF control system is shown in Fig. 2, which includes the feedback control loops for amplitude control and phase control. By comparing the pick-up signal with the reference value, the program in the FPGA can adjust the output signal to compensate the deviation and thus make the system stable.

3.1 Hardware of the control system

The local oscillator (LO) is one of the most important parts in the above system. An HP Signal Generator 8663 A is used to generate 1.3 GHz RF signal, which can be mixed with the 30.72 MHz signal generated by an Agilent Function Generator 33250 A to get an LO signal with 1330.72 MHz [8]. An internal reference signal with a frequency of 10 MHz can ensure that both generators work on the same locked phase.

The other important part is the clock distribution scheme. We use a reference signal with a frequency of 30.72 MHz for the reference clock (CLK) of AD9510. The central frequency of the voltage controlled oscillator (VCO) of AD 9510 is 245.76 MHz, and we can obtain eight route signals, four with a frequency of 122.88 MHz for ADC and FPGA, and the other four with 245.76 MHz for DAC.

The advanced Stratix IV GX FPGA Development Kit [9] is chosen for development because of its outstanding performance. Compared with the former products, the Stratix IV series adopts a low power consumption production process, has high performance and high density, which efficiently improves the operation speed and the interior max clock frequency. The daughter board analog-to-digital and digital-to-analog (ADDA) data conversion Terasic P0035 with dual high-speed 150 MSPS A/D and 250 MSPS D/A channels is chosen for its high sampling rate.

3.2 Internal algorithm of the FPGA

The internal algorithm of the FPGA, as shown in Fig. 3, is used in our system. The amplitude and phase information are abstracted from the IF signal through (In-phase) and Q (Quadrature) sampling and the CORDIC algorithm. Comparing them with the reference value, deviations of amplitude and phase are obtained and used to adjust the amplitude and phase

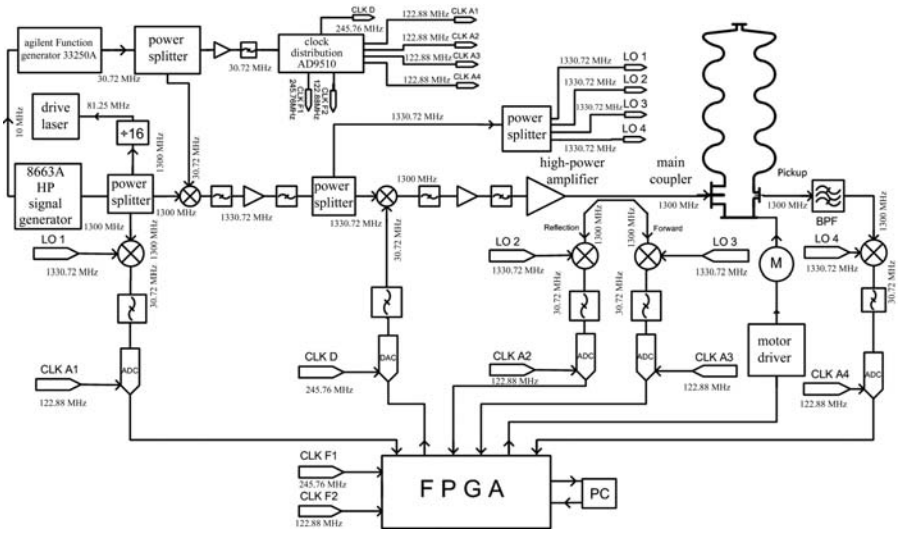

Fig. 2. The schematic of the control system for a PKU SRF photocathode injector.

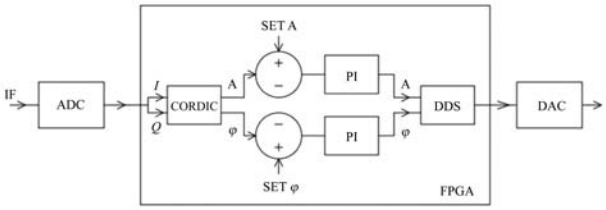

Fig. 3. Internal algorithm of the FPGA.

of input signal. The PI controller is used to make the deviation signals proper for adjustment and the DDS rebuilds the sine signal. Finally, through DAC, such a series of digital signals are converted to analog signals. Therefore, the amplitude and phase of RF signal can be kept within a small range.

IQ sampling has been widely used in the LLRF control system because of the advantage that the signals are orthogonal and do not interfere each other. The IF signal from down-conversion is sampled by the ADC to obtain a series of signal: I, Q, $-I$, $-Q$.... as shown in Fig. 4.

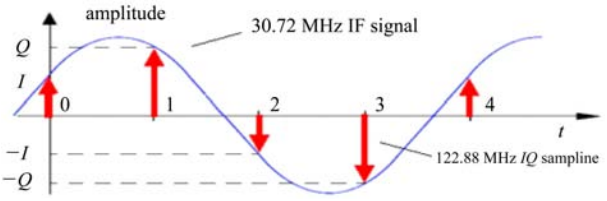

Fig. 4. The IQ sampling sketch map.

IQ signal can be converted to amplitude and phase form through the CORDIC algorithm based on coordinate rotation in a plane. I and Q are regarded as the initial components $[X_0, Y_0]$ of a vector. Rotating this vector with an angle of α_i=arctan (2^{-i}) each time until y-component tends to 0, amplitude is the value of x-component of the final vector, while phase can be expressed as $\theta = \sum_0^{n-1} \sigma_i \alpha_i, \sigma_i \in \{-1, 1\}$, here σ_i indicates the direction of rotation and is decided by the quadrant where the vector is.

4 Disturbance analysis

Several disturbances or system errors influencing the precise capability of the LLRF control system are analyzed as follows.

Period-jitter is one parameter to describe the clock quality that influences the final precision of the whole system [10]. It is usually defined as the time difference of a measured cycle period from an ideal cycle period. The phase-offset caused by period jitter is related to IF signal [11] as Formula (2):

$$\Delta\varphi = 360^\circ \cdot \Delta t \cdot f_{\mathrm{IF}}. \tag{2}$$

In our system, the jitter of the ADC sampling period is approximately 2 ps (rms), considering f_{IF}=30.72 MHz, the phase error caused by the period jitter is 0.022°.

For digital processes, it is imperative to lead quantization noise to system. The main source of quantization noise is the conversion from analog signal to digital signal. The resolution ratio of our ADDA conversion board is 14 bits and there are 13 effective bits. Therefore, the phase errors caused by ADC conversion are 0.008° (rms).

Data interception is often used to save the memory of FPGA or get more proper data bits for the next step. In our system, 32 data bits containing the phase information are intercepted to data with 13 bits

as the address of direct digital synthesis (DDS) [12], which inevitably causes a certain amount of disturbance. In general, 13 bits correspond to the phase precision of 0.044°.

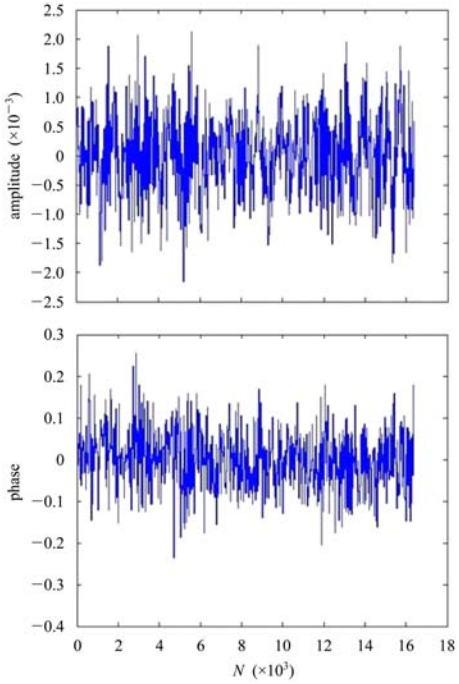

Fig. 5. Short-term stability of amplitude and phase.

In addition, non-linearity of devices, phase noise from generator, temperature drift, etc. are also disturbances influencing the precise capability of the LLRF control system. In our design, 8663 A and 33250 A are selected to reduce the disturbance because the phase drift can be suppressed by using low phase-noise signal generators. The harmonic wave caused by non-linear devices is suppressed by a surface acoustic wavefilter, which has the advantage of high attenuation of the stop band and a steep edge of the pass band.

We maintained the room temperature in a certain range to suppress the temperature drift caused by active devices.

5 Experiment and preliminary results

The experiment for the feedback operation was performed on a 3.5 cell superconductive cavity at room temperature. As shown in Fig. 5, the preliminary results of the stability of amplitude and phase subtracting deviation signal is within ±0.2% and ±0.2°, respectively in short term. The results approached the requirement of design closely, but more efforts are being still made in an attempt to improve the precision of the LLRF system in order to achieve the goal of ±0.1% for amplitude and of ±0.1° for phase stability.

6 Conclusion

For the stable operation of the DC-SC photocathode injector, a digital low level control system has been designed. Through careful design of control loops, careful choice of hardware and suppressing the disturbances causing phase error, the control precision of our LLRF system should achieve the requirement of ±0.1% for amplitude and of ±0.1 ° for phase stability. Now the system is being tested and will be used for the operation of the DC-SC injector in the near future.

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