# A high-precision multi-channel TAC and QAC module for the neutron detection wall *

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**Abstract:** A single width NIM module that includes eight channels of the time-to-amplitude converter (TAC) and the charge-to-amplitude converter (QAC) is introduced in the paper, which is designed for the large neutron wall detector to measure charge (energy) and time interval simultaneously. The module adopts a high precision gated integration circuit to realize TAC and QAC. The input range of TAC is from 30 ns to 1 μs, and the input range of QAC is from 40 pC to 600 pC. The linearity error of TAC is lower than 1.28%, and the time resolution of TAC is less than 0.871%. The linearity error of QAC is lower than 0.81%, and the resolution of QAC is better than 0.936%.

**Key words:** time-to-amplitude, charge-to-amplitude, neutron detection wall, multi-channel

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## 1 Introduction

With the national scientific project of the Cooling Storage Ring of the Heavy Ion Research Facility (HIRFL-CSR) built in Lanzhou, the External Target Facility (ETF) for HIRFL-CSR is also under construction. The neutron wall is a key detector of the ETF [1], and it is used to measure neutrons with energies from several tens of MeV to 1 GeV.

The neutron wall detector is a large detector array which is composed of 252 detection units, and the time-of-flight method is used to detect neutrons [2]. The start detector at the front of the neutron wall produces the start signal of the time-of-flight, and the neutron wall detector produces the stop signal of the time-of-flight. The block diagram of this eight-channel NIM module is shown in Fig. 1; it includes time-to-amplitude converter (TAC) circuits, charge-to-amplitude converter (QAC) circuits, discriminators and signal splitters.

After being discriminated, the start signal triggers the TAC circuit to start integration and the QAC circuit to prepare for integration. After being split, on the one hand, the stop signal after being discriminated and shaped triggers the TAC circuit to stop integration, so that the time interval between the start and stop signal is converted to a proportional voltage. On the other hand, the stop signal is sent into the QAC circuit, and is converted into a proportional voltage on the integration capacitor after a current splitter. The voltage amplitude which is formed by the TAC and QAC is converted to a digital signal by the data acquisition system after multiplexer.

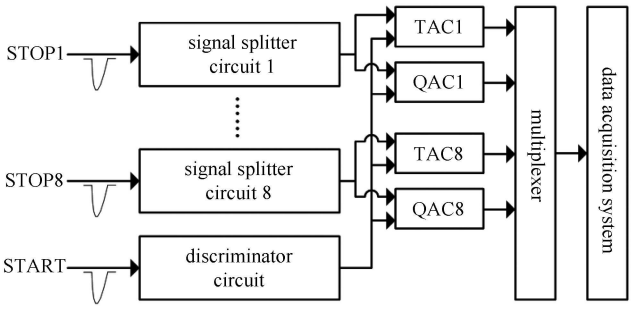


Fig. 1. Block diagram of the eight-channel module.

## 2 The design of TAC

The TAC technique is widely used in the time-of-flight spectrometer at present [3]. Realization of TAC is to convert the time interval into a proportional voltage. After initial tests, the time interval, between the START signal given by the start time detector at the front of the reaction target and the STOP signal which is the stop sign of flight time of the neutron given by the neutron wall detector, is about 200 ns. So with careful study and comparison [4], a new TAC circuit, a start-stop type TAC, has been proposed which is constructed based on a high precision constant current source and the gated

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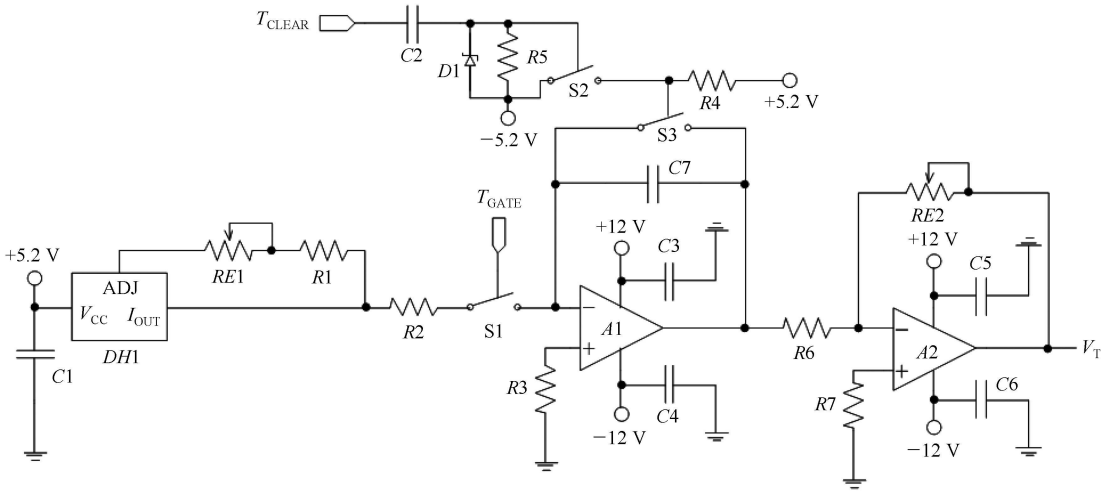


Fig. 2. Circuit diagram of TAC.

integration. It is characterized by simple circuit structure, high conversion precision, fast discharging, and so on.

The integrating and amplification circuit of the TAC unit is mainly composed of a constant current source circuit, gated integration circuit and amplifier. The circuit diagram is shown in Fig. 2. The general idea is that we use a gated integration to convert the current from a constant current source into voltage, and the integration time named $T_{\rm GATE}$ is the time interval between the START and STOP signal. The voltage will be maintained for the data acquisition system. Then a control signal named $T_{\rm CLEAR}$ discharges the voltage on capacitor $C7$.

The constant current source circuit consists of $C1$, $DH1$, $RE1$, and $R1$. $DH1$ is a constant current source device which has good voltage stability and temperature stability, and the current stability is from 0.02 %/V to 0.05 %/V. The temperature coefficient ($\alpha$MAX) is from $1.0\times10^{-4}$/℃ to $3\times10^{-4}$/℃. This circuit can steadily output current from 0.3 mA to 25 mA by adjusting the potentiometer $RE1$. In order to prevent the potentiometer from adjusting to zero, it should be connected to a small resistor $R1$ behind $RE1$.

The high-speed DMOS analog switches S1, S2 and S3, FastFET Op Amps $A1$ and $A2$, the integration capacitor $C7$, three resistors $R3$, $R4$ and $R5$, one diode $D1$, three capacitors $C2$, $C3$, and $C4$ are used to compose the gated integration circuit with the reset function. When $T_{\rm GATE}$ is high, S1 is closed; when $T_{\rm CLEAR}$ is high, S2 is closed, and S3 is opened. The main function of this part is integrating current from the constant current source and maintaining the output voltage. A high-performance mica capacitor $C7$ is used as the integration capacitor, $C2$ for the effective isolation of constant voltage, the $C3$, and $C4$ for decoupling capacitors.

If one single switch, for example S3, is used, $C7$ cannot be discharged successfully, especially for negative voltage. In order to discharge $C7$ completely, the substrate voltage of switch S3 is set to minus 5.2 V. However, it is not possible to switch the S3 on or off directly by a signal from CPLD in this case.

A driven type DMOS switch circuit is designed, which is composed of two switches S2 and S3, two resistors $R4$ and $R5$, and one diode $D1$. The control signal from CPLD drives the switch S2 on or off, which can make the control voltage of switch S3 changes from positive 5.2 V to negative 5.2 V. This means the control voltage of S3 is 5.2 V when the S2 is switched off, otherwise the control voltage of S3 is minus 5.2 V when S2 is switched on. This circuit can ensure S3 is cut-off or turned-on completely, so that the gated integration circuit can work properly. The inverting amplifier consists of operation amplifier $A2$, resistors $R6$, $R7$ and $RE2$, and the gain can be changed by adjusting the $RE2$.

A leading-edge timing discriminator is designed to discriminate the signal from the detector for time analysis. The leading-edge timing circuit of the START signal is shown in Fig. 3. The circuit includes a new fast discrimination device MA1. The START signal is first fed into the fast isolation circuit, and then enters the leading-edge timing circuit in order to ensure the consistency of the signal delay. Test results indicate that the propagation delay of the entire leading-edge timing circuit is less than 1 ns; the time walk range is about 4 ps and 6 ps in theory. This circuit has greatly improved the precision of TAC.

The integration time ($T_{\rm GATE}$) in the TAC circuit is determined by the input signals START and STOP. The duration between START and STOP is the amount of time to be converted. The START and STOP signals are converted to TTL signals by a leading-edge timing circuit

and then sent into a CPLD; the CPLD produces a $T_{\rm GATE}$ signal and a $T_{\rm CLEAR}$ signal. The falling-edge of $T_{\rm RANG}$ generates the control signal of the multiplexer and the sampling clock signal $\rm SAMP_{CLK}$. The $\rm SAMP_{CLK}$ controls correspondingly the data acquisition card to read out the voltage signals of eight channels TAC and eight channels QAC. Fig. 4 shows the timing chart of the TAC operation.

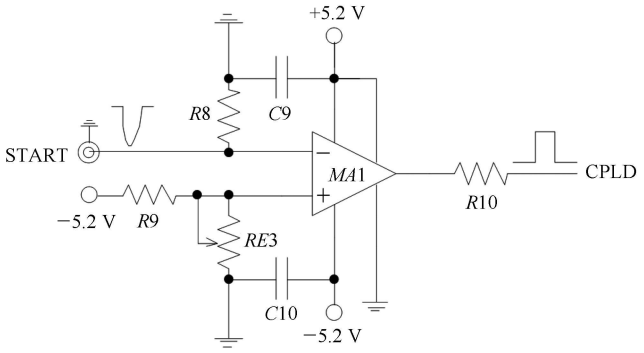


Fig. 3. Leading-edge timing circuit of START.

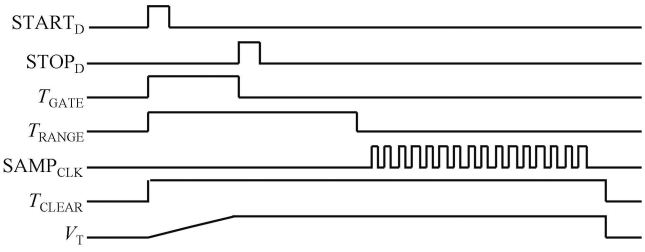


Fig. 4. Timing chart of TAC operation.

$\rm START_D$ and $\rm STOP_D$ signals, which are from START and STOP, and formed by the leading-edge timing circuit, correspond to the integration start time and stop time. $\rm START_D$ and $\rm STOP_D$ in CPLD are formed into the switch control signal ($T_{\rm GATE}$) of the integration, and its width is the time interval to be measured. The charged voltage on the integration capacitor $C7$ is given by Eq. (1):

$$V_{\rm T}=\frac{I(T_{\rm STOP}-T_{\rm START})}{C7}=\frac{IT_{\rm GATE}}{C7}. \tag{1}$$

$T_{\rm RANGE}$ is triggered by the $\rm START_D$ and set as the maximal input range of TAC to be measured. $\rm SAMP_{CLK}$ which is triggered by $T_{\rm RANGE}$ and sent to the data acquisition system is a sample clock for the TAC and QAC module with eight channels. $T_{\rm CLEAR}$ is triggered by the $\rm START_D$ and used as clear signal, when it is driven high, the switch is closed.

## 3 The design of QAC

The output signal from the neutron wall detector is very fast. If we use a charge sensitive preamplifier to process the signal, it will cause a very long trailing edge. So it is not suitable when the count rate of the input signal is high. Therefore we developed a QAC approach to realize fast and accurate QAC based on previous work by Inaba et al [5, 6], and its prominent characteristic is the fast conversion speed, large range of input signal (40–600 pC), high precision, low power, high integration, simple circuit structure and operation stability. The QAC circuit mainly consists of a current splitter circuit, gated integration circuit and amplifier. The gated integration circuit and amplifier are the same as the one in the TAC unit; the structure of the QAC circuit is shown in Fig. 5.

The gated integration circuit can be charged on the integration capacitor by controlling the analog switch with an input charge (current) after the rapid current splitter circuit. It can obtain voltage amplitude proportional to the input signal on the integration capacitor.

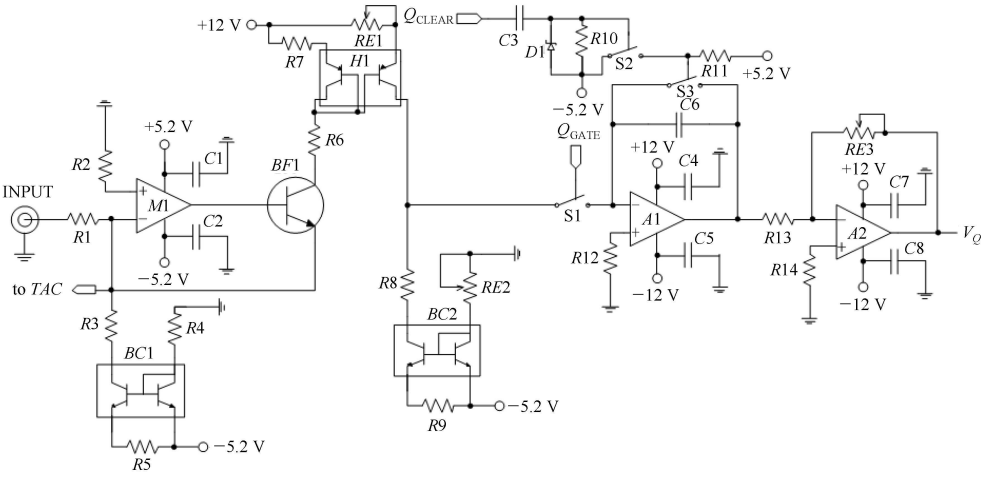


Fig. 5. Circuit diagram of the QAC.

After sampling, the voltage amplitude will be discharged by the discharge switch, so that the potential at each endpoint of the capacitor returns to the initial state.

$M1$, $BC1$, $BC2$, $BF1$, and $H1$ compose the fast current splitter circuit, and we choose a wide band amplifier $M1$ and the transistor $BF1$ with cut-off frequency up to 3 GHz, which can improve the sensitivity of the input circuit as well as the signal-to-noise ratio, and achieve impedance transformation. The micro-current source consists of $R3$, $R4$, $R5$, and $BC1$, which can realize precise current adjustments. It can compensate offset current on the negative input of the amplifier $M1$, and also ensure the input is zero potential and zero current in cooperation with the negative feedback circuit when no signal is input. Another current source consists of $R8$, $R9$, $RE2$ and $BC2$, which ensures that the input of the gated integration is zero current by adjusting $RE2$ when no signal is input, and the output pedestal voltage is completely eliminated. The current mirror consists of $R7$, $RE1$, and $H1$. As long as changing the proportional relationship of the $RE1$ and $R7$, the ratio of the input current and the current fed to the gated integration can be changed. In this way, it can initially amplify the small current signal and improve signal-to-noise ratio. If the input signal is a big current signal, it can be attenuated down by this current mirror. So this fast current splitter circuit can function as an attenuation network, which simplifies the circuit structure, and can greatly improve measurement accuracy and measurement range.

Figure 6 shows the timing chart of the QAC operation. $\mathrm{START_D}$ is a common signal for TAC and QAC, the STOP signal is the output of the detector, $Q_{\mathrm{GATE}}$ signal is triggered by the $\mathrm{START_D}$, the width of $Q_{\mathrm{GATE}}$ can be set in the program according to the actual condition, which must include the pulse duration of the STOP signal to ensure that STOP was completely integrated. $Q_{\mathrm{CLEAR}}$ is also triggered by $\mathrm{START_D}$. When all output signals of the eight channels of TAC and QAC have been sampled, the $Q_{\mathrm{CLEAR}}$ is driven to low-level to discharge the voltage on the integration capacitor.

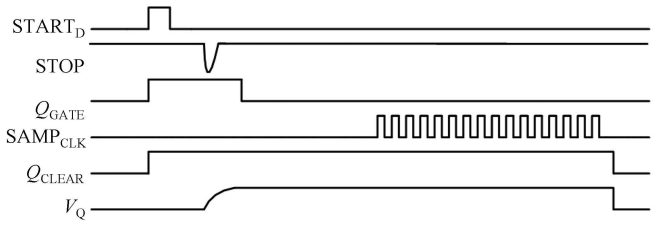


Fig. 6. Timing chart of QAC operation.

When the leading-edge of $Q_{\mathrm{GATE}}$ signal is coming, the normally open switch S1 is closed, the normally closed switch S2 is opened, the system begins to work, and the STOP signal is integrated. When the falling-edge of the $Q_{\mathrm{GATE}}$ signal is coming, the normally open switch S1 is opened, the DAQ system begins to acquire data from all the channels of this system, and the state of the normally closed switch S2 is unchanged at the same time. When all signals of the channels have been acquired, the normally closed switch S2 is closed, the integration capacitor is discharged, and then this system begins to prepare for the next data acquisition.

## 4 Performance

In order to test the function of this NIM module, we set up a test system in the experimental field, the block diagram of which is shown in Fig. 7. The system has been tested with cosmic rays for a period of 30 days with non-stop work. In this system, a NI PXI-6133 card is employed as a data acquisition card.

The TAC and the QAC have a common start and work at the same time. The result is shown in Figs. 8 and 9. The symbol 'Entries' is the count of events, the symbol 'Mean' is the average voltage, and the symbol 'RMS' is the standard deviation of the amplitude. The test results conform to the Gaussian distribution.

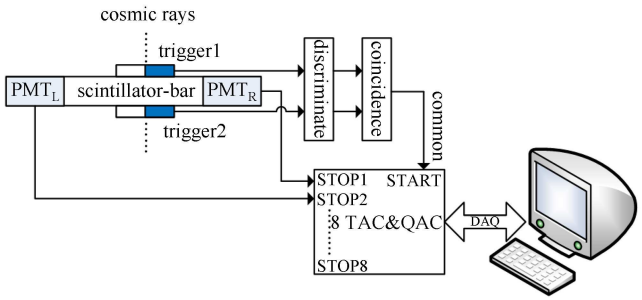


Fig. 7. Block diagram of functional test system.

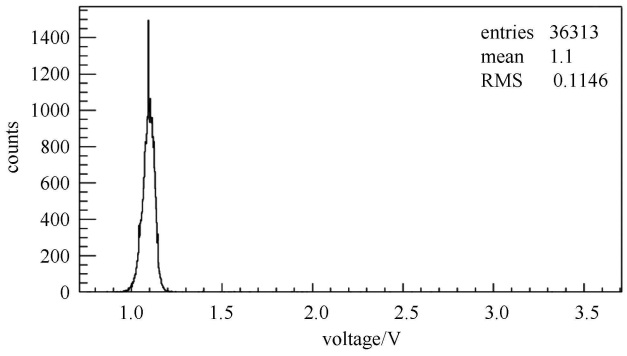


Fig. 8. Functional test result of TAC.

The performance of this NIM module was tested in the laboratory with a Phillips CAMAC Model 7120 as the signal source, a NI Corporation DAQ card PXI-6133 and an industrial computer were used to compose the data acquisition system.

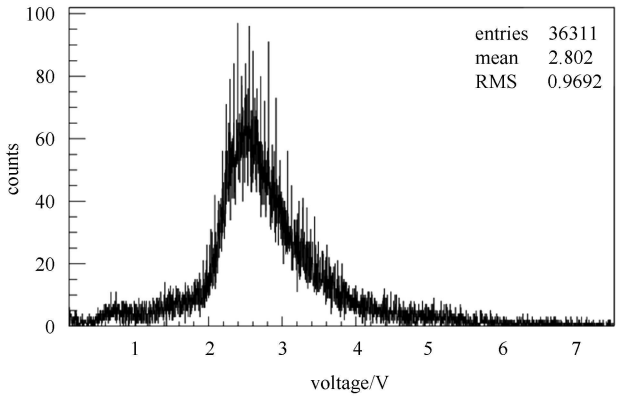


Fig. 9. Functional test result of QAC.

Table 1. Parameters of the TAC.

| type | parameter value |
|---|---|
| measurement range | 30 ns to 1 μs |
| holding capacitor | 1.33 nF |
| full scale differential output | 10 V (±5V) |
| discharge time | <200 ns |
| output voltage noise | <4.6 mV (rms) |
| output offset voltage | <±4.1 mV |
| linearity error | 0.051% to 1.280% |
| time resolution | 0.066% to 0.871% |
| absolute resolution | 261 ps to 656 ps |

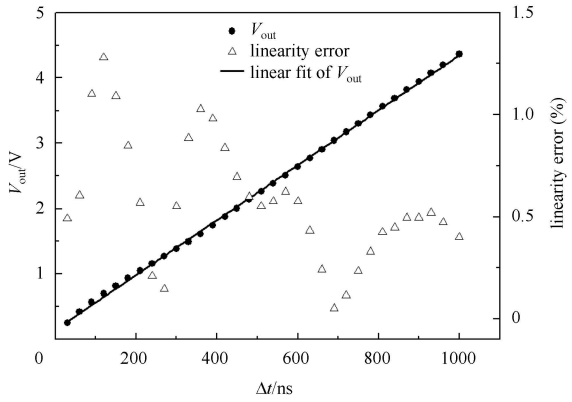


Fig. 10. Transfer curve and linearity errors of TAC.

Parameters of the TAC and the QAC are shown in Tables 1 and 2; each test point includes more than 10 million events. The transfer curve and linearity errors of TAC are shown in Fig. 10. The longer the time interval under test, the better the resolution. The transfer curve and linearity errors of QAC are shown in Fig. 11. The higher the input charge, the better the resolution.

Table 2. Parameters of the QAC.

| type | parameter value |
|---|---|
| measurement range | 40 pC to 600 pC |
| holding capacitor | 330 pF |
| full scale differential output | 10 V (±5V) |
| discharge time | <200 ns |
| output voltage noise | <5.2 mV (rms) |
| output offset voltage | <±4.7 mV |
| linearity error | 0.003% to 0.810% |
| energy resolution | 0.043% to 0.936% |
| absolute resolution | 240 fC to 374 fC |

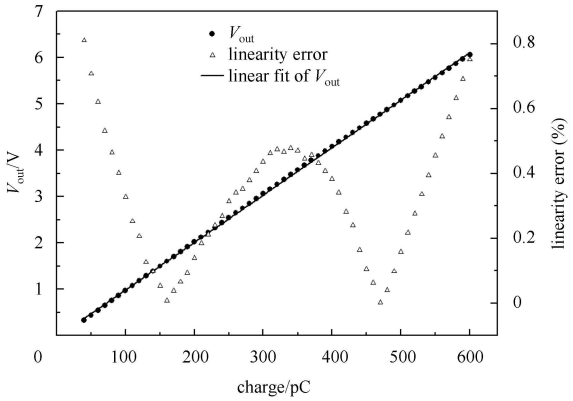


Fig. 11. Transfer curve and linearity errors of QAC.

## 5 Summary

This NIM module and a normal DAQ system are used to constitute a TDC and QDC system, and a comparison test has been implemented. When the Phillips CAMAC Model 7120 is chosen as the signal source, the performance of this system is superior to some commercial TDC and QDC modules; the linearity error and resolution of this NIM module are little better than the commercial CAMAC module. The characteristics of the TAC and QAC circuits are a high processing speed, simple circuit structure, high precision and low power dissipation, and also a low manufacture cost. In particular, this NIM module can read out the time interval and charge information simultaneously with the same signal. The resolution and linearity error are a little worse at the very low measurement range, which needs to be improved. This module can be used widely to construct a front-end read-out electronics system for large array detectors.

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