# Application of the DRS4 chip for GHz waveform digitizing circuits *

YANG Hai-Bo(杨海波)[1,2] SU Hong(苏弘)[1;1)] KONG Jie(孔洁)[1] CHENG Ke(成科)[1,3]
CHEN Jin-Da(陈金达)[1] DU Cheng-Ming(杜成名)[1,2] ZHANG Jing-Zhe(张惊蛰)[1,2]

[1] Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou 730000, China
[2] University of Chinese Academy of Sciences, Beijing 100049, China
[3] Northwest Normal University, Lanzhou 730070, China

**Abstract:** A new fast waveform sampling digitizing circuit based on the domino ring sampler (DRS), a switched capacitor array (SCA) chip, is presented in this paper, which is different from the traditional waveform digitizing circuit constructed with an analog to digital converter (ADC) or time to digital converter. A DRS4 chip is used as a core device in our circuit, which has a fast sampling rate up to five gigabit samples per second (GSPS). Quite satisfactory results are acquired by the preliminary performance test for this circuit board. Eight channels can be provided by one board, which has a 1 V input dynamic range for each channel. The circuit linearity is better than 0.1%, the noise is less than 0.5 mV (root mean square, RMS), and its time resolution is about 50 ps. Several boards can be cascaded to construct a multi-board system. The advantages of high resolution, low cost, low power dissipation, high channel density and small size make the circuit board useful not only for physics experiments, but also for other applications.

**Key words:** DRS4, waveform sampling, digitizing circuit, high sampling rate, high resolution

**PACS:** 29.40.mc, 84.30.-r, 84.37.+q **DOI:** 10.1088/1674-1137/39/5/056101

## 1 Introduction

The maximum information of a pulse from a detector can be acquired by the experimenter by digitizing a fast signal directly, for example, the drift time and pulse area can be easily obtained from the waveform [1]. Traditionally, a flash analog to digital converter (ADC) is used for digitization [2, 3]; however such systems suffer from sampling rates in the range from about 50 to 250 MHz with 10 or 12 bit resolution, low channel densities, huge power consumption and are usually expensive. Due to the development of component technology, an alternative approach is to utilize switched-capacitor arrays (SCA) [4–6]. The input signal is sampled and stored in a series of capacitors at high sample rates under the control of a shift register, and digitized with a commercial ADC operating at a lower sample rate.

In our design, a DRS4 [7], the fourth version chip of DRS, is chosen. Because the domino wave runs continuously in a ring, the chip is called a domino ring sampler (DRS). The DRS from the Paul Scherrer Institute in Switzerland is a typical SCA [8]. Because of the high channel density of the DRS system, it becomes affordable for waveform digitization in experiments in which ADCs or time to digital converters are currently used. This technique has been developed for particle physics applications. At present, it has been realized using switched capacitor circuits, for example MAGIC [9] and MEG [10]. It also can be useful for other applications, such as PET scanners and portable oscilloscopes.

A prototype of a waveform sampling readout board based on the DRS4 chip has been developed, and preliminary tests implemented. The DRS4 waveform digitizing board records the input signal with a high sample rate between 0.7 and 5 GS/s. Its gain can be adjusted to match different kinds of detector signals. The input dynamic range of the waveform digitizing board is about 66 dB at a sample rate of 5 GS/s, and the time resolution is about 50 ps.

The key parameters of the waveform digitizer are as follows:

1) Input bandwidth $\geqslant$ 650 MHz;
2) 1 V input dynamic range;
3) 16 bit DAC calibration;
4) Up to 5 GS/s sampling rate;
5) Digital trigger logic and external trigger implemented in the field programmable gate array (FPGA);
6) 14 bit ADC resolution;

Received 4 August 2014
* Supported by National Natural Science Foundation of China (11305233), Specific Fund Research Based on Large-scale Science Instrument Facilities of China (2011YQ12009604)
1) E-mail: suhong@impcas.ac.cn

7) Serial DRS4 readout;
8) Readout multiplexed and speed up to 33 MHz;
9) Board to board communication.

## 2 Design of the waveform digitizing board

### 2.1 DRS4 technology and operation

The DRS4 chip is fabricated by a 0.25 mm 1P5M MMC process and is a radiation hard SCA. DRS4 has up to 5 GHz sampling speed, 9 differential input channels per chip, 11.5 bit vertical resolution, and 4 ps timing resolution [11]. The waveform is stored in 1024 sampling cells per channel, and can be readout after sampling with a commercial ADC at 33 MHz sampling rate. The range of the sampling rate is from GHz to the MHz. The time stretch ratio (TSR) is given as shown in Eq. (1). Dead time is described by Eq. (2).

$$\mathrm{TSR}\equiv\delta t_{\mathrm{s}}/\delta t_{\mathrm{d}}, \tag{1}$$

$$\text{dead time}=\text{Sampling Window}*\mathrm{TSR}, \tag{2}$$

where, $\delta t_{\mathrm{s}}$ is the sampling interval of DRS4, $\delta t_{\mathrm{d}}$ is the sampling interval of readout ADC.

For example, typical values are: $\delta t_{\mathrm{s}}$=0.5 ns (2 GSPS), $\delta t_{\mathrm{d}}$=30 ns (33 MHz), sampling window=100 ns, the result of TSR=60, dead time=100 ns×60=6 μs.

The main parameters of the DRS4 chip are shown in Table 1.

Table 1. DRS4 chip main parameters.

| type | parameter value |
|---|---|
| power supply | single 2.5 V |
| sampling speed | 700 MS/s to 5 GS/s |
| analog channel | 8+1 |
| storage depth | 1024 cells |
| high SNR | ∼69 dB |
| low noise | ∼0.35 mV |
| analog outputs | multiplexed or parallel |
| channel or chip cascading | yes |
| readout mode | full or region of interest |
| inputs bandwidth | 950 MHz |

The DRS4 chip consists of an on-chip series of inverters generating a sampling frequency in the GHz range. A sampling signal propagates through these inverters freely (domino principle). There is an analog voltage supplied to the chip, then transmission gates between these inverters make the sampling frequency controllable in a wide range. The frequency of the domino wave is stabilized by a phase locked loop and defined by an external reference clock. The differential input signal is stored in 150 fF capacitors. The domino wave runs continuously in a circular fashion, but the domino wave can be stopped at any sampling cell by a trigger signal. The trigger signal stops the domino wave, and then analog contents of the sampling cells are read out under the control of a shift register, and digitized by an external ADC simultaneously. Fig. 1 shows the simplified schematic of the chip.

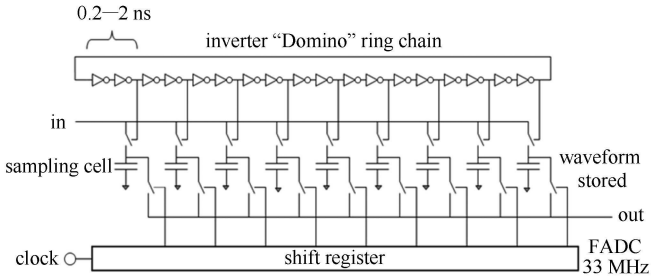


Fig. 1. Simplified schematic of the DRS4 chip.

The DRS4 chip has three kinds of waveform readout modes [10]. A feature of the DRS4 chip is its transparent mode, whereby with this mode, the analog input to the DRS4 chip is digitized and applied to the analog output at the same time. In the full readout mode, all 1024 sampling cells are read out consecutively starting from cell 0 with 1024 clock cycles for external digitization. In the region of interest readout mode, it can read only a subset of all sampling cells, and the dead time is reduced. The DRS4 chip has a sampling depth of 1024 cells per channel. For the applications to obtain deeper sampling depth, it supports cascading of two or more channels on one chip, and several DRS4 chips can even be daisy-chained.

### 2.2 Circuit design

#### 2.2.1 Overview of the waveform sampling digitizing board

The overview of the waveform sampling digitizing board is shown in Fig. 2. The circuit consists of a DRS4 chip, an ADC chip, an FPGA and other devices. The digitizing board has eight analog channels. The DRS4 chip is capable of sampling differential input channels, so the single-end inputs terminated by 50 Ω need to be converted into differential signals, which is achieved by active buffers chosen. The on-board 16-bit DAC generates reference voltages to measure the offsets of all sampling cells for calibration, and generates offset voltages for DRS4 and buffers. The calibration information of the board is stored in an electrically erasable programmable read-only memory (EEPROM). The input signal has a 1 V maximum amplitude, and the AC coupled mode is adopted at inputs. The data in DRS4 is read by an FPGA and a 14-bit commercial ADC. The control of the digitizing board, receiving outputs of ADC and com-

municating with a personal computer (PC), are implemented entirely by an FPGA. A low-end FPGA from Xilinx Spartan 3 families is selected as the FPGA in the central control unit [12]. The data and commands are transmitted between a PC and digitizing board via a universal serial bus (USB), the connection between the digitizing board and PC is implemented with a USB controller. The data transfer rate of the USB is over 20 MB/s. A comparator is used in each analog input channel for generating a triggering signal. One input of the comparator comes from the non-inverting input of the differential inputs of DRS4, and for the other one, a programmable level is set as a reference. After comparison, a trigger signal is generated by the comparator. These trigger signals from all comparators can be combined into "AND" or "OR" logic in the FPGA, and then a trigger is generated by the FPGA. Once the trigger is effective, the sampling in the DRS chip is stopped and the information stored in the SCA is digitized with an external ADC at a sampling rate of 33 MHz. A prototype of the waveform sampling digitizing board, as shown in Fig. 3, is realized, and can be used to construct a small data acquisition system.

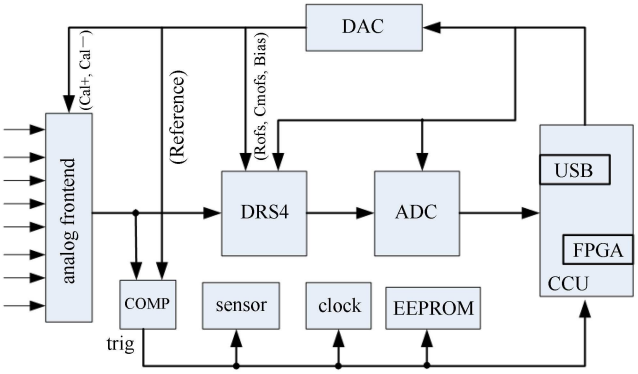


Fig. 2. Block diagram of a waveform sampling digitizing board.

### 2.2.2 Analog frontend

Figure 4 illustrates the schematic of the analog frontend. As the inputs of DRS4 are differential signals, a wideband, fully-differential operational amplifier THS4508, from Texas Instruments®, is chosen as the differential driver [13]. The bandwidth of the amplifier reaches 2 GHz. The current given by the THS4508 for driving a DRS4 is about 1 mA. An analog switch ADG901, from Analog Devices®, is placed at the front end of THS4508, which is dc-coupled with the input of THS4508. When the DRS4 is calibrated, this switch is switched off, the input of the circuit is isolated. An AC coupling mode is applied to the inputs of DRS4 and ADG901; the advantage is that it can protect the input devices and simplify the processing for common mode levels. As the NMOS transistors at the inputs of DRS4 show a nonlinear behavior, and the linearity becomes a little worse at the portions near the rails, it is recommended to be operated within the entire linear range. The input baseline is generated by a DAC to map input signals, which can apply an individual DC offset to the differential input lines. Because the analog frontend is used for processing high speed analog signals, some detailed methods are adopted for designing a printed circuit board, such as matched impedance, separate power supply and proper termination. The analog frontend circuit is simulated by PSpice. The three dB bandwidth of the analog frontend is about one GHz when the load of circuit is a 10 pF capacitance.

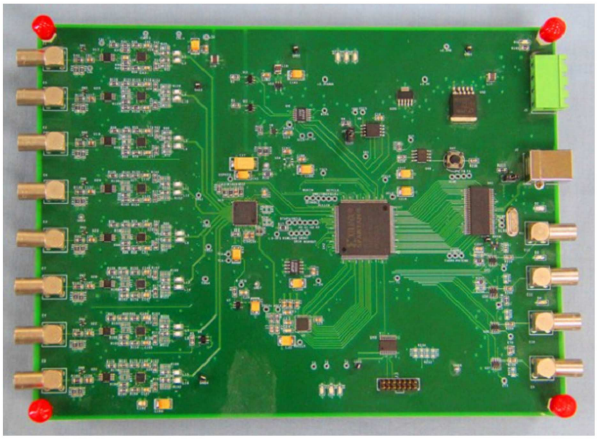

Fig. 3. (color online) Prototype of the waveform sampling digitizing board.

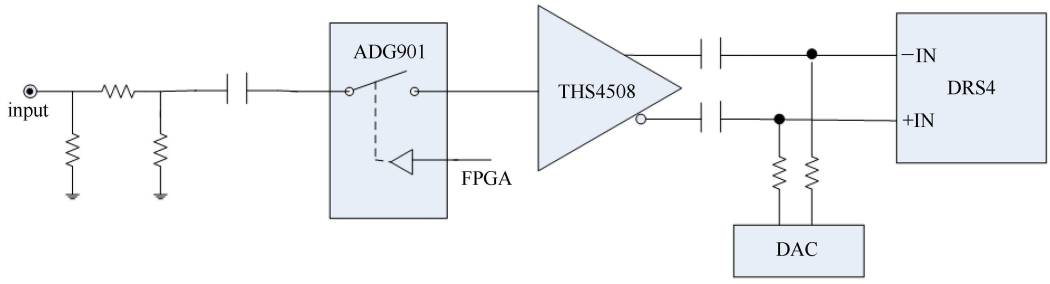


Fig. 4. Schematic of the analog frontend.

2.2.3 Digitization

All DRS4 channels are read out one by one for digitization, so an ADC is required. There is a very strict phase relationship between the DRS4 readout clock and the ADC clock. The phase relationship of the two clocks must be fixed and about 10 ps jitter tolerated for the best linearity, and a delay circuit is designed for generating a phase shifted clock with a low jitter. The signal to noise ratio (SNR) of the DRS4 is 66 dB after offset correction. In order to get the optimal performances of the waveform sampling readout board, a 14-bit ADC from Analog Devices is used.

2.2.4 Control voltages and calibration

In order to let the DRS4 chip operate normally, certain configuring voltages are needed, such as DC offset, BIAS, ROFS and O-OFS. BIAS and O-OFS can be set internally by the DRS4 itself, and also can be set externally by supplying a bias voltage. In our design, an external 16-bit DAC is used to generate a bias voltage connected to these control lines. The bias voltage can be fine-tuned to compensate for variations of the chip. This DAC also provides threshold voltage to the inverting input (input-) of the comparator; when one event comes, this comparator can output a trigger signal to the FPGA. These control voltages are shown in Fig. 5. A 0 V calibration voltage offered by a 16-bit DAC is sent to all DRS4 inputs for the voltage calibration. Because more driving current is required for driving inputs of the DRS4, a low noise Op Amp AD8605 [14] is employed as a buffer after the DAC. A calibration test point is measured and an offset voltage and gain are evaluated. As parameters of transistors in the chip gradually change normally, the timing calibration is necessary. In order to reduce nonlinearity, we need to measure the delay of each cell. An internal 240 MHz clock is sampled by one channel of the DRS4, and the deviation between the expected period and the measured period is used to determine the effective width of each cell. This design ensures the jitter of timing calibration is less than 20 ps. The values of calibration voltage and calibration timing data are saved in an EEPROM.

2.2.5 Multi-board configuration

The waveform sampling digitizing board can be used for a detector that has multiple detection cells. Several waveform sampling digitizing boards can be cascaded, and a multi-board system, supplying multiple analog input channels, is constructed. The multi-board configuration is shown in Fig. 6. There are four control inputs on each board, Trigger IN, Trigger OUT, Clock IN and Clock OUT. The port "Trigger IN" accepts an external trigger when a hit event is coming, which is much like a trigger of an oscilloscope. The port "Trigger OUT" sends the pulse with a fixed width to the "Trigger IN"

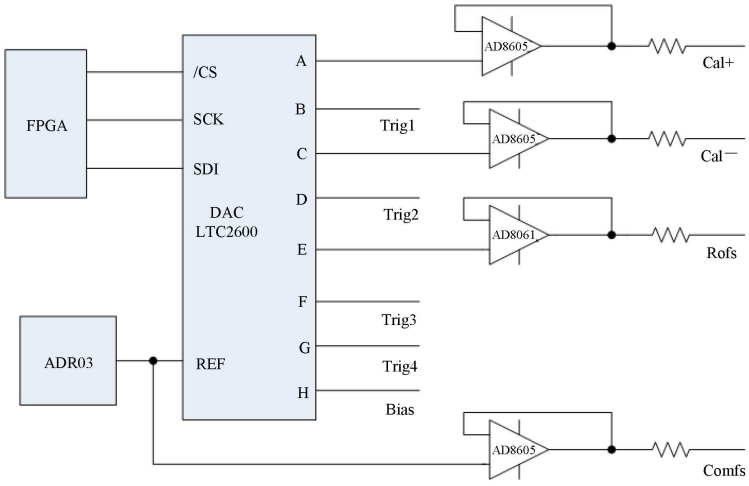


Fig. 5. The circuit for producing control voltages.

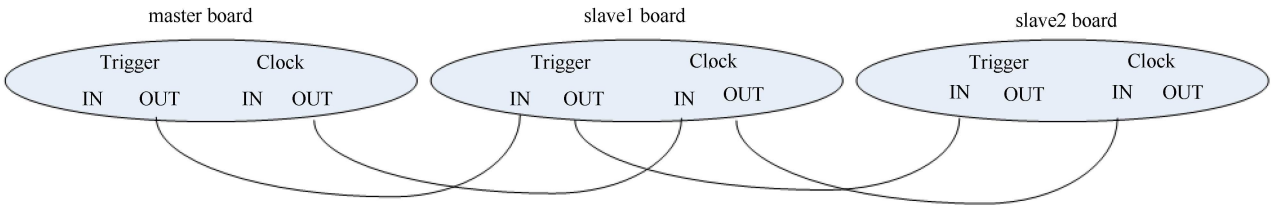


Fig. 6. Scheme of multi-board configuration.

port on the next board. The "Clock IN/OUT" ports allow a better synchronization among different boards for multi-board configuration. Both the trigger and the clock signals are passed by a daisy-chain mode from the master board to the slave board. In this system, more than eight input channels are read out for each event. The data from different boards can be distinguished by the board number.

## 3 Test and results

The preliminary test of the prototype board was implemented, and the results of the measurement are discussed in this section.

### 3.1 Baseline noise

The RMS noise on the baseline is measured before offset correction, and also measured after offset correction. Because of some factors caused by integrated circuit manufacture technology, each sampling cell in SCA has a fixed residual voltage (i.e. DC offset). The DC offset basically is fixed for the sampling cell, but has some differences among the different sampling cells. If the DC offset is not corrected, it can cause nonlinear distortion to the reconstruction of the waveform. Therefore, DC offset of each sampling cell is needed to be calibrated and removed from the sampling result. In the calibration, a 0 V voltage, generated by the 16-bit DAC, is given to each input channel of DRS4. Statistical analysis of the sampled results is performed for all the sampling cells. Fig. 7(a) shows a 0 V DC signal sampled at 5 GS/s sampling rate before offset and gain correction, which shows a noise level of 7.3 mV RMS. Fig. 7(b) shows a 0 V DC signal sampled at 5 GS/s sampling rate after offset and gain correction; the noise level is reduced significantly to about 0.5 mV RMS. So the "fixed pattern" offset error of 7.3 mV RMS can be reduced to 0.5 mV RMS by offset correction implemented in FPGA. Thus, for $1V_{\rm peak-peak}$ dynamic input range, the SNR is about 66 dB (1 V linear range / 0. 5 mV).

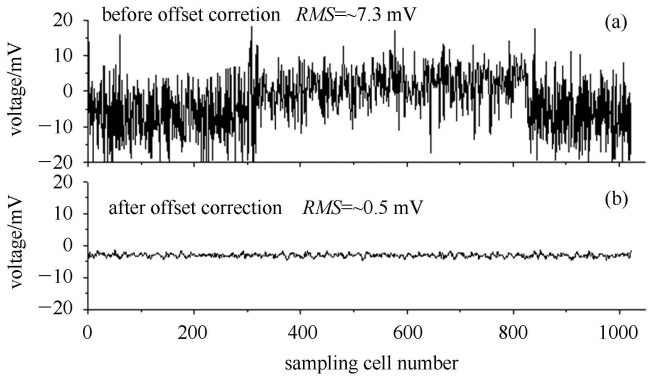


Fig. 7. (a) 0 V DC signal sampled at 5 GS/s before offset correction; (b) 0 V DC signal sampled at 5 GS/s after offset correction.

Another measure method of the SNR is to obtain the effective number of bits (ENOB) [15]. For an input sine wave signal with the specified frequency and amplitude, ENOB is defined by Eq. (3)

$$ENOB=\log_2\left(\frac{FSR}{NAD\sqrt{12}}\right)\approx N-\log_2\left(\frac{NAD}{\varepsilon_Q}\right), \quad (3)$$

where $N$ is the number of bits digitized, $FSR$ is the full-scale range of the recorder, $NAD$ is the noise and distortion, $\varepsilon_Q$ is the $RMS$ ideal quantization error.

In the test, a sine wave signal is generated, which has a peak-peak value of about 0.45 V, and the frequency is 20 MHz. Fig. 8 gives a typical result, $NAD$=1.31 mV, $\varepsilon_Q$=2 V$\times 2^{-14}/\sqrt{12}$=3.524$\times 10^{-5}$. These values are brought into Eq. (3), then:

$ENOB$=14$-\log_2$ (1.31/0.035)=14$-$5.2=8.8 bits.

In addition, another measurement for the input signal frequency of 150 MHz is also implemented. Following the description in reference [15] and Eq. (3), the ENOB has been obtained for the DRS4 readout system, and is 8.1 bits.

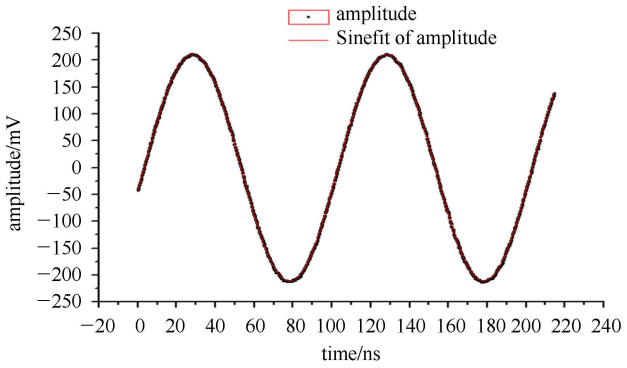


Fig. 8. (color online) Reconstruction of 10 MHz sine wave signal sampled at 5 GS/s.

### 3.2 Amplitude nonlinearity

The amplitude nonlinearity is measured by using the pulse signals with 1 MHz frequency generated by AFG3252 [16]. The amplitude of the input signal is adjusted from $-$400 mV to +400 mV, the step adjusted each time is 100 mV. Input signals are sampled with 5 GHz sampling rate, and the amplitudes of the signals are read out with 33 MHz sampling rate. The linearity of one channel of the digitizing board is shown in Fig. 10, and the amplitude nonlinearity is about 0.1%. Fig. 9 also shows output residuals deviating from the linear fit values after offset and gain calibration. The error points are the maximum deviation values.

Typical detector signals are shown in Fig. 10, sampled by the DRS4 chip with the 2 GHz sampling rate.

An experimental test is implemented using two identical detector modules. Each detector module consists of a 5.2 cm×5.2 cm×1.5 cm LYSO scintillation crystal matrix (composed of 8×8 pixel finger crystals) coupled to the Hamamatsu H8500 PMT wrapped in Teflon. Two LYSO scintillation detector units are separated 16 cm away from each other, and $^{22}$Na source is placed between them as a positron source [17]. Each H8500 has sixty-four anode signals, the 64 anode signals are divided by an external voltage divider board consisting of resistor chains. The sixty-four anode signals can be sent out individually via two $x$ and two $y$ electrodes. The outputs of the voltage divider board offer energy information, and dynode 12 of the H8500 PMT offers time information. Results on energy and timing information are shown as an example in Fig. 10, including two time signals and four energy signals.

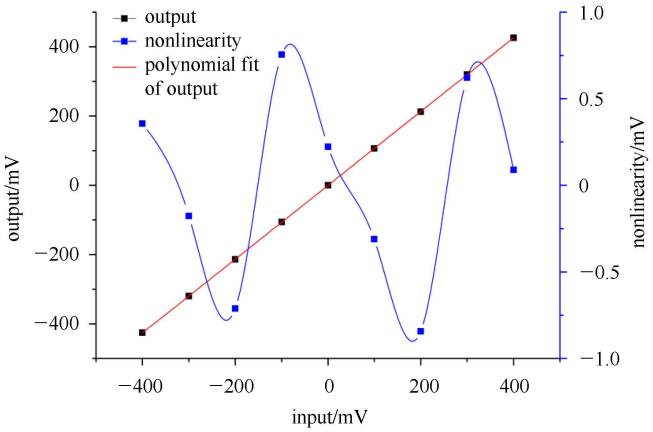


Fig. 9. (color online) Analog output versus analog input, and residuals deviating from the fit value, typical nonlinearity after offset and gain calibration.

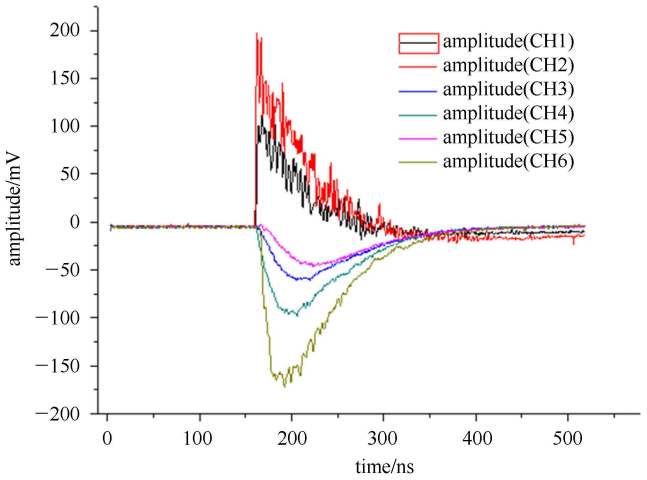


Fig. 10. (color online) Waveforms of the two time signals (positive) and four energy signals produced by DRS4.

### 3.3 Precision of timing measurement

In the DRS4 chip, because of the possible variation of the delay interval of the inverter gate, the "delay interval width" of each sampling cell is different, and therefore needs to be measured and calibrated. An internal 240 MHz clock is sampled by one channel with a 5.12 GHz sampling rate. The delay interval of each sampling cell is obtained and shown in Fig. 11.

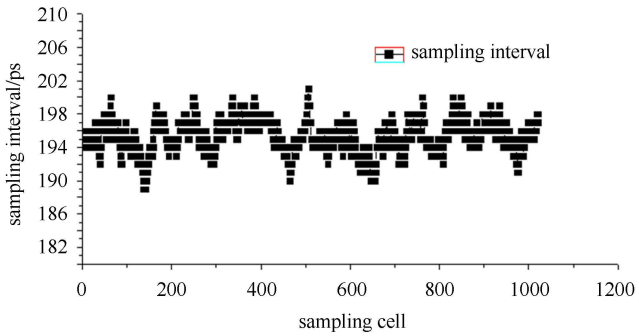


Fig. 11. DRS4 delay interval of each sampling cell.

There are a variety of methods to calibrate the "delay interval width". We use the "cross zero of sine" method. For the same sampling interval, a steeper slope at the sampling point will decrease the effect caused by error of amplitude. The signal distortion also affects the measurement results of ENOB. However, reliable ENOB measurement is a challenge for a DRS4 board, since the "delay interval width" of the DRS4 chip is different. This causes significant signal distortion if the sample points are treated as being uniformly spaced in time. More sophisticated calibration and less timing jitter are expected to improve the measurement results of ENOB.

The precision of the timing measurement is studied by a delay time measurement based on a cable delay method. The cable delay method aims to eliminate time jitter of the signal generator itself. A pulse signal from the signal generator AFG3252 [16] is split and fed into

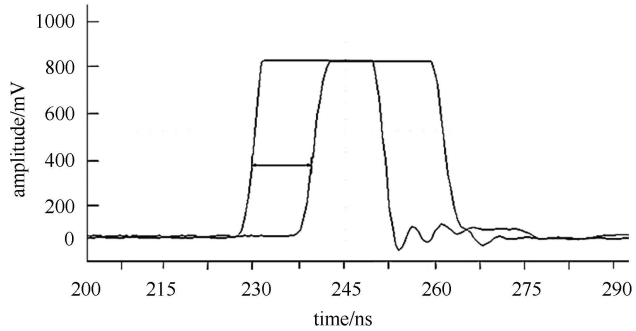


Fig. 12. Pulse of two-channel signals.

two channels with a fixed cable delay between them. A fixed 9.28 ns delay time is offered by one cable. Tests are performed, and two pulses output from two channels of the DRS4 are shown in Fig. 12. The distribution of delay intervals tested is shown in Fig. 13, and the sigma of delay time spectrum is 52 ps.

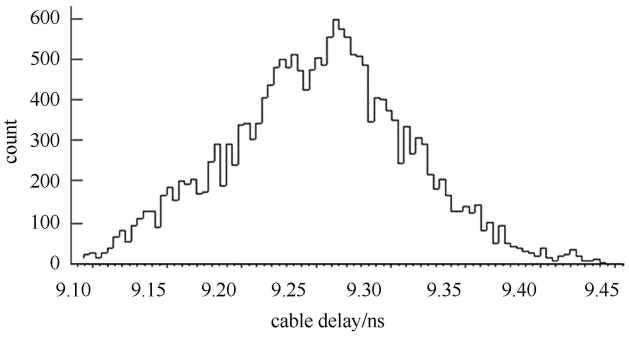


Fig. 13. Distribution of cable delay times tested.

## 4 Conclusions

A new flexible waveform sampling readout digitizing board, based on the DRS4 chip, is realized and tested. The sampling rate for an input signal can be changed from 700 MHz to 5 GS/s, and the sampling rate of ADC for readout digitization is 33 MHz. The bandwidth (−3 dB) of the digitizing board is about 700 MHz, the input dynamic range is one volt. The SNR is about 66 dB, and the time resolution is approximately 50 ps. A high speed sampling based on SCA is combined with an ADC with lower sampling rate but high precision, which gives the system the features of high resolution, low cost, low power dissipation, high channel density and small size. It can replace some digitizing systems based on flash ADC for waveform digitization. It is very useful for a waveform digitizing system with multiple input channels. The waveform sampling readout digitizing board can be employed to construct data acquisition systems for other applications as well.

## References

1 WANG J H, ZHAO L, FENG C Q et al. Nucl. Sci. Technol., 2012, **23**(2): 109–113
2 Dhawan S, Hughes V W, Kawall D et al. Nucl. Instrum. Methods A, 2000, **450**(2): 391–398
3 Kornilov N V, Khriatchkov V A, Dunaev M et al. Nucl. Instrum. Methods A, 2003, **497**: 467–478
4 Haller G M, Wooley B A. IEEE Trans. Nucl. Sci., 1994, **41**: 1203–1207
5 Kleinfelder S. IEEE Trans. Nucl. Sci., 1990, **37**(3): 1230–1236
6 Delagnes E, Degerli Y, Goret P et al. Nucl. Instrum. Methods A, 2006, **567**: 21–26
7 Ritt S. IEEE Nuclear Science Conference Record, 2008. 1512–1515
8 Ritt S, Dinapoli R, Hartmann U. Nucl. Instrum. Methods A, 2010, **623**(1): 486–488
9 Baixeras C. arXiv preprint astro-ph/0403180, 2004
10 Mori T. PSI R-99-05 MEG Experiment Proposal. Paul Scherrer Institute, 1999
11 Paul Scherrer Institute. DRS4 Datasheet, 2009. http:www.psi.cn
12 Xilinx Corporation. Application Note, 774 (v.1.2), 2006. http:www.xilinx.com
13 Texas Instruments Incorporated, THS4508 Datasheet, 2008. http:www.TI.com
14 Analog Devices, AD8605 Datasheet, 2009. http:www.analog.com
15 IEEE Standards. IEEE Std 1057-2007, IEEE Standard 1057, 2007
16 Tektronix Corporation. AFG3252 User Guide, 2008. http:www.tek.com
17 CHEN J D, XU H S, HU Z G et al. Chin. Phys. C, 2011, **35**(1): 61