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Investigation on a solution to improve the irradiation reliability of SOI NMOSFET

YU Wen-Jie(俞文杰)[1)] ZHANG Zheng-Xuan(张正选) HE Wei(贺威) TIAN Hao(田浩)
CHEN Ming(陈明) WANG Ru(王茹) BI Da-Wei(毕大伟) ZHANG Shuai(张帅) WANG Xi(王曦)

(The State Key Laboratory of Functional Materials for Informatics Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China)

Abstract A solution is developed to improve the irradiation reliability of SOI NMOSFET (N-type Metal Oxide Semiconductor Field Effect Transistor). This solution, including SOI (Silicon On Insulator) wafer hardening and transistor structure hardening, protects the SOI circuit from total dose irradiation effect.

Key words SOI, irradiation, total dose effect, NMOSFET

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1 Introduction

SOI (silicon on insulator) devices are mostly employed in integrated circuits under irradiation environment due to its intrinsic immunity to transient irradiation effect. But it deteriorates seriously under total dose irradiation[1]. While buried oxide sharply reduces charge collection volume, it brings a leakage path when irradiated[2—5]. This reliability issue is more suffered by NMOSFET (N-type Metal Oxide Semiconductor Field Effect Transistor) transistor as the positive charges formed in buried oxide invert the n-type back channel of NMOSFET. Another effect is caused by the side parasitic transistor, which should also be concerned under total dose irradiation[6]. The problem is raised from the positive trapped charges in field oxide and they may induce an inversion layer at the bird's beak, giving rise to leakage current paths from the drain to the source.

Aiming at those two irradiation effects, we have developed a solution including two key processes. The first one is to harden the SOI wafer by Si ion implantation. After Si ion implantation, the irradiation hardness of the buried oxide is improved. PL (Photo Luminescence) method provides an evidence of the mechanism. The second is the special structure, named "edgeless", utilized in NMOSFET layout, which cuts off the leakage path due to side parasitic transistor. Comparison after irradiation between the edgeless transistor and the conventional one shows the effectiveness of the edgeless structure.

2 Side parasitic transistor

Side parasitic transistor is a typical irradiation effect of NMOSFET. A conventional NMOSFET and its leakage path through side parasitic transistor are shown in Fig. 1(a). In our solution, the transistor structure shown in Fig. 1(b) is employed. Its edgeless property eliminates the leakage path through the bird's beak.

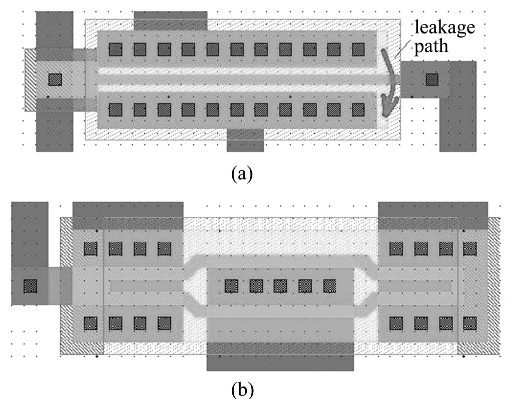

Fig. 1. Layout of (a) the conventional transistor and (b) the edgeless transistor characteristics.

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1) E-mail: casan@mail.sim.ac.cn

Transistors with both structures are irradiated by X-ray. Their back gate characteristics are shown in Fig. 2. It is clearly seen that there is a bump existing in the curve of conventional transistor, because of the effect of side parasitic transistor. The current contributed by the side parasitic transistor overlaps the normal drain current and induces considerable leakage current when the back gate voltage is zero. We can also see in Fig. 2 that the edgeless transistor is immune from that effect as the leakage path is cut off.

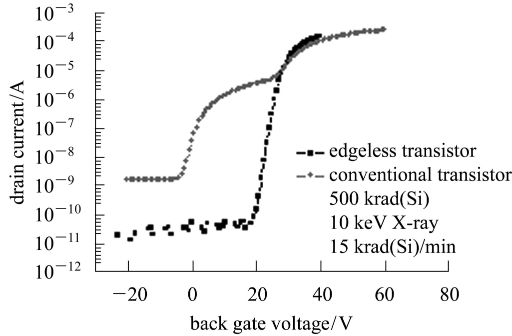

Fig. 2. Back gate sub-threshold characteristic after irradiation dose of 500 krad (Si).

3 Buried oxide

Buried oxide is a unique region of SOI device. The trapped charges formed during the irradiation in this region may induce considerable leakage current between the drain and the source. The response of NMOSFET fabricated on conventional SOI substrate after irradiation is shown in Fig. 3. The transistor has the structure in Fig. 1(b), so no side parasitic transistor effect is observed.

Figure 3(a) shows the back gate characteristics after irradiation. It is seen that the back gate threshold voltage shifts obviously after irradiation. When the back gate voltage is zero, the back channel is still inverted, inducing high leakage current. The front gate characteristics are shown in Fig. 3(b). With the dose increasing, the transistor suffers higher leakage current when the gate voltage is zero. This effect directly results from the inversion of back channel[7].

To protect the transistors from this effect, we have developed a hardening method by Si ion implantation and anneal. The hardening process includes implanting Si ion into the SOI substrate at specific dose and annealing the substrate at a specific circumstance.

We fabricated transistors in hardened substrate. Its response after irradiation is shown in Fig.4. An accident during test spoiled the integrity of the curve at pre-irradiation case but it still can be seen in Fig. 4(a) that the back gate threshold voltage shifts much less for the hardened sample. At the dose of 1 Mrad (Si),

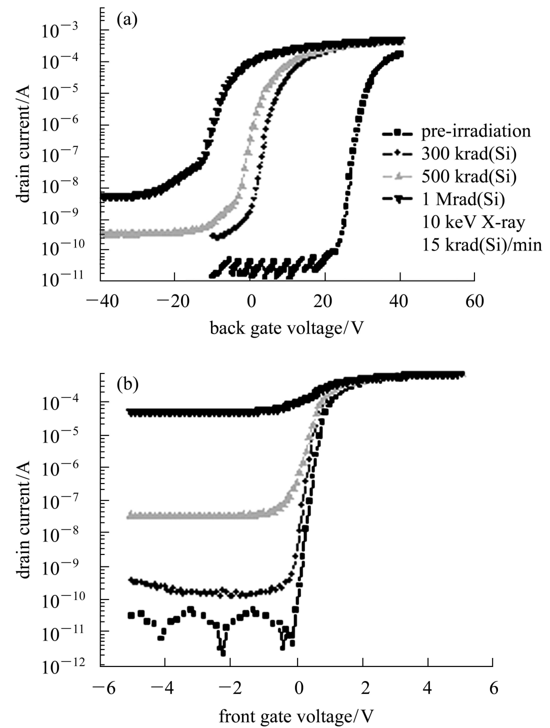

Fig. 3. Back gate (a) and front gate (b) subthreshold characteristics of the transistor fabricated on the unhardened SOI wafer after irradiation.

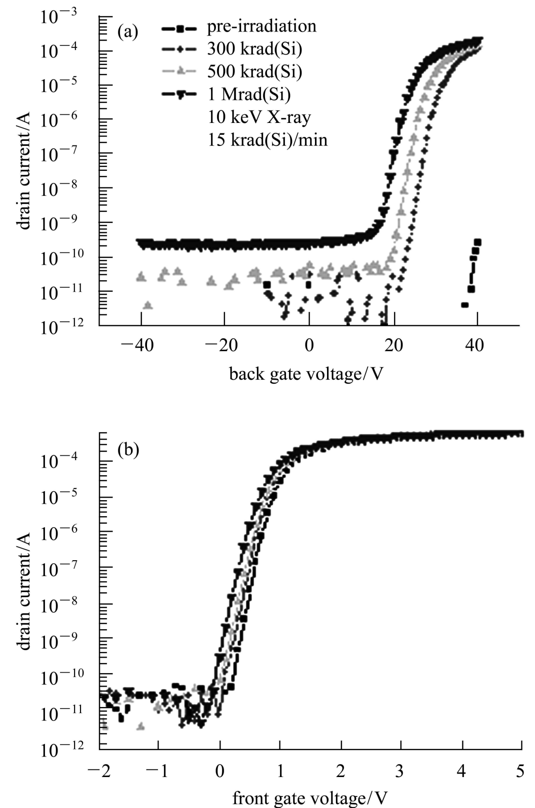

Fig. 4. Back gate (a) and front gate (b) subthreshold characteristics of the transistor fabricated on the hardened SOI wafer during irradiation.

the back threshold voltage shifts less than 25 V on 10^{-6} A basis, compared with the unhardened sample shifting more than 40 V. As to Fig. 4(b), the front gate characteristic nearly shows no deterioration because the back channel has not been inverted.

4 Discussion

To explain the mechanism of the hardening effect by Si ion implantation and anneal, we investigate in what have been changed or created in oxide after this process. It has been reported that Si ion implantation into oxide may form Si nanostructure, which can act as electron traps[8]. So we wonder whether there exists Si nanostructure after our hardening process. PhotoLuminescence (PL) method is utilized.

We acquired PL spectra of both unhardened and hardened samples, shown in Fig. 5. The spectra of hardened oxide feature a band peak at nearly about 750 nm[9], compared with the flat spectra of unhardened oxide. The characteristic PL band of Si nanostructure peaking at 730 nm has been reported. So we believe that the band peak at 750 nm can be an evidence to prove that the Si nanostructure is formed in oxide after the hardening process. The Si nanostructure works as electron trap and traps electrons to compensate positive charges induced by irradiation.

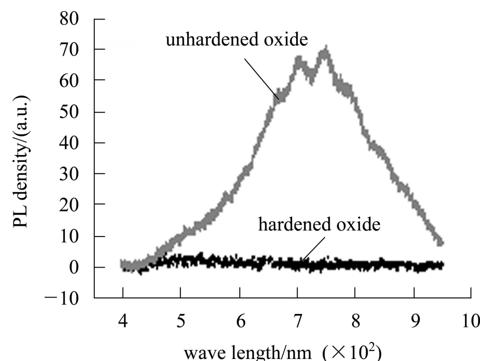

Fig. 5. PL spectra of the hardened and unhardened oxide.

5 Conclusion

This work develops a solution to protect the SOI device from irradiation, including edgeless structure and buried oxide hardening. Both processes prove valid by experiment and the solution is expected to be utilized to improve the irradiation reliability of SOI integrated circuit.

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